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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,727	12/28/2001	Stefan Johannes Bitterlich	9824-0077-999	2597

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EXAMINER	
PHU, PHUONG M	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/040,727	**Applicant(s)** BITTERLICH ET AL.	
	Examiner Phuong Phu	**Art Unit** 2611	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 09 March 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-37.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: SEE ATTACHMENT.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

3/24/06

PHUONG PHU
PRIMARY EXAMINER

Phuong Phu
Primary Examiner
Art Unit: 2611

ATTACHMENT

This Attachment is responsive to the Applicant's Response filed on 3/9/06.

The applicant mainly argues that neither of Subramanian et al (2002/0015401), hereafter referred Subramanian I, and Subramanian et al (2002/0031166), hereafter referred Subramanian II, discloses the channel CODEC processor as claimed, wherein the channel CODEC processor has processor core(s), that provides an algorithm-specific kernel block with configuration data wherein the processor core(s) is/are located in the channel CODEC processor, and algorithm specific kernel block(s) which is/are located within the channel CODEC processor.

The examiner respectfully disagrees. Note that the rejections are based on the limitations given in the claims.

-It is deemed that Subramanian I discloses the channel CODEC processor, the processor core(s) and algorithm specific kernel block(s), as claimed. The explanation is following.

Regarding to claims 1-15, Subramanian I discloses a channel CODEC processor (100, 121) (see figure 1B), which is considered here equivalent (EQ) with the claimed limitation "channel CODEC processor", wherein Subramanian I channel CODEC processor comprises:

an algorithm-specific kernel block (102a, 104) (see figure 1B), (EQ with the claimed limitation "algorithm-specific kernel block") wherein Subramanian I algorithm-specific kernel block is operable to receive a data stream (122), the kernel block comprising logic (104) tailored to perform at least one step of a channel CODEC algorithm on the data stream (see [0039-0041]; and

a processor core (112, 121) (see figure 1B), (EQ with the claimed limitation "processor core"), wherein Subramanian I processor core is coupled to provide configuration data (121) to

the algorithm-specific kernel block, the configuration data causing the kernel block to perform the at least one step of the channel CODEC algorithm according to one of a plurality of wireless communication standards (e.g., TDMA standards (see [0037]) as specified by the configuration data (121) (see figures 1B, 1D, and [0037, 0042, 0043, 0051, 0053]).

Regarding to claims 16-21, Subramanian I discloses a channel CODEC processor (100, 121) (see figure 1B), which is considered here equivalent (EQ) with the claimed limitation "channel CODEC processor", wherein Subramanian I channel CODEC processor comprises:

a first algorithm-specific kernel block (comprising (418)) (see figure 4), (EQ with the claimed limitation "first algorithm-specific kernel block", wherein Subramanian I first algorithm-specific kernel block is comprised in device (104) (see figure 1B) and operable to receive a data stream outputted from device (404), the first algorithm-specific kernel block comprising logic (418) tailored to perform a step "Viterbi" decoding of a first channel CODEC algorithm on the data stream to generate a first processed data stream (see [0153-0159]);

a second algorithm-specific kernel block (422) (see figure 4), (EQ with the claimed limitation "second algorithm-specific kernel block", wherein Subramanian I second algorithm-specific kernel block is comprised in device (104) (see figure 1B) and coupled to the first algorithm-specific kernel block to receive the first processed data stream, the second algorithm-specific kernel block comprising logic (422) tailored to perform a step "CRC" of a second channel CODEC algorithm on the first processed data stream to generate a second processed data stream (see [0155]); and

a processor core (112, 121) (see figure 1B)), (EQ with the claimed limitation "processor core"), wherein Subramanian I processor core is coupled to provide configuration data (121) to

the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel CODEC algorithm and the step of the second channel CODEC algorithm according to one of a plurality of wireless communication standards, (e.g., TDMA standards (see [0037]), as specified by the configuration data (see figures 1B, 1D, and [0037, 0042, 0043, 0051, 0053]).

Regarding to claims 22-28, Subramanian I discloses a channel CODEC processor (100, 121) (see figure 1B), which is considered here equivalent (EQ) with the claimed limitation "channel CODEC processor", wherein Subramanian I channel CODEC processor comprises:

a plurality of processor cores (102a, 108) (see figure 1B), (EQ with the claimed limitation plurality of processor cores"), wherein Subramanian I plurality of processor cores includes a first processor core (102a) and a second processor core (108) operable to process data in a data stream outputted from device (129 or 128) (see [0035-0044]); and

a plurality of algorithm-specific kernel blocks (410, 406) (see figure 4), (EQ with the claimed limitation "plurality of algorithm-specific kernel blocks"), wherein Subramanian I plurality of algorithm-specific kernel blocks are comprised in device (104) (see figure 1B) and include a first algorithm-specific kernel block (410) and a second algorithm-specific kernel block (406) (see figure 4) coupled to the first processor core and the second processor core, respectively, wherein the first algorithm-specific kernel block is operable to receive first data from the first processor core and to perform at least one step (410) of a first channel CODEC algorithm on the first data, wherein the second algorithm-specific kernel block is operable to receive second data from the second processor core and to perform at least one step (406) of a second channel CODEC algorithm on the second data (see [0153-0159]).

Regarding to claims 29-32, Subramanian I discloses a channel CODEC processor (comprising (104, 112, 121)) (see figure 1B), which is considered here equivalent (EQ) with the claimed limitation "channel CODEC processor", wherein Subramanian I channel CODEC processor comprises:

a first algorithm-specific kernel block (410) (see figure 4), (EQ with the claimed limitation "first algorithm-specific kernel block"), wherein Subramanian I first algorithm-specific kernel block is comprised in device (104) (see figure 1B) and operable to receive a demodulated data stream from device (102a) (see figure 1B), the kernel block comprising logic tailored to perform at least one step (410) of a channel decoding algorithm on the demodulated data stream (see [0153-0159]); and

a first processor core (121, 112) (see figure 1B), (EQ with the claimed limitation "first processor core"), wherein Subramanian I first processor core is coupled to provide first configuration data (121) to the algorithm-specific kernel block, the configuration data causing the kernel block to perform the at least one step of the channel decoding algorithm according to one of a plurality of wireless communication standards (e.g., TDMA standards (see [0037]), as specified by the configuration data (see figures 1B, 1D, and [0037, 0042, 0043, 0051, 0053]).

Regarding to claims 33-37, Subramanian I discloses a channel CODEC processor (comprising (104, 112, 121)) (see figure 1B), which is considered here equivalent (EQ) with the claimed limitation "channel CODEC processor", wherein Subramanian I channel CODEC processor comprises:

a first algorithm-specific kernel block (418) (see figure 4), (EQ with the claimed limitation "first algorithm-specific kernel block", wherein Subramanian I first algorithm-

specific kernel block is comprised in device (104) (see figure 1B) and is operable to receive demodulated data stream from device (102a) (see figure 1B), the first algorithm-specific kernel block comprising logic tailored to perform a step (418) of a first channel decoding algorithm on the demodulated data stream to generate a first processed data stream (see [0153-0159]);

a second algorithm-specific kernel block (422) (see figure 4), (EQ with the claimed limitation "second algorithm-specific kernel block", wherein Subramanian I second algorithm-specific kernel block is comprised in device (104) (see figure 1B) and coupled to the first algorithm-specific kernel block to receive the first processed data stream, the second algorithm-specific kernel block comprising logic tailored to perform a step (422) of a second channel decoding algorithm on the first processed data stream to generate a second processed data stream (see [0155]); and

a first processor core (121, 112) (see figure 1B), (EQ with the claimed limitation "first processor core"), wherein Subramanian I first processor core is coupled to provide first configuration data (121) to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel decoding algorithm and the step of the second channel decoding algorithm according to one of a plurality of wireless communication standards (e.g., TDMA standards (see [0037]), as specified by the configuration data (see figures 1B, 1D, and [0037, 0042, 0043, 0051, 0053]).

-With similar reasons set forth for claims 1-37 as being anticipated by Subramanian I, it is deemed that Subramanian II discloses the channel CODEC processor, the processor core(s) and algorithm specific kernel block(s), as claimed (see Subramanian II, figures 1B, 1D and 4), since both Subramanian I and Subramanian II teach similar subject matters which are deemed

that they disclose the channel CODEC processor, the processor core(s) and algorithm specific kernel block(s), as claimed.

3/24/06
Phuong Phu

PHUONG PHU
PRIMARY EXAMINER